*New Product*

MITSUBISHI LSIs

# M5M44265CJ,TP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 4194304-BIT ( 262144-WORD BY 16-BIT ) DYNAMIC RAM

## DESCRIPTION

This is a family of 262144-word by 16-bit dynamic RAMs with Hyper Page mode fuction,fabricated with the high performance CMOS process, and is ideal for the buffer memory systems of personal computer graphics and HDD where high speed, low power dissipation,and low costs are essential. The use of double-layer metalization process technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self or extended refresh current is low enough for battery back-up application. This device has 2$\overline{CAS}$ and 1$\overline{W}$ terminals with a refresh cycle of 512 cycles every 8.2ms.

## FEATURES

| Type name | $\overline{RAS}$ access time (max.ns) | $\overline{CAS}$ access time (max.ns) | Address access time (max.ns) | $\overline{OE}$ access time (max.ns) | Cycle time (min.ns) | Power dissipation (typ.mW) |
|---|---|---|---|---|---|---|
| M5M44265CXX-5,5S | 50 | 13 | 25 | 13 | 90 | 625 |
| M5M44265CXX-6,6S | 60 | 15 | 30 | 15 | 110 | 550 |
| M5M44265CXX-7,7S | 70 | 20 | 35 | 20 | 130 | 475 |

XX=J,TP

- Standard 40 pin SOJ,44 pin TSOP( II )
- Single 5V±10% supply
- Low stand-by power dissipation
  - CMOS Input level ---------- 5.5mW(Max)
  - CMOS Input level ---------- 550 μW(Max) *
- Operating power dissipation
  - M5M44265Cxx- 5,5S ---------- 688mW (Max)
  - M5M44265Cxx- 6,6S ---------- 605mW (Max)
  - M5M44265Cxx- 7,7S ---------- 523mW (Max)
- Self refresh capability*
  - Self refresh current ---------- 150 μA(max)
- Extended refresh capability
  - Extended refresh current ---------- 150 μA(max)
- Hyper page mode (512-column random access), Read-modify-write,$\overline{RAS}$-only refresh,$\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.
- Early-write mode,$\overline{OE}$ and $\overline{W}$ to control output buffer impedance
- 512 refresh cycles every 8.2ms (A0 ~A8)
- 512 refresh cycles every128ms (A0~A8)*
- Byte or Word control for Read/Write operation (2$\overline{CAS}$,1$\overline{W}$ type)

* :Applicable to self refresh version(M5M44265CJ, TP -5S, -6S,-7S :option) only

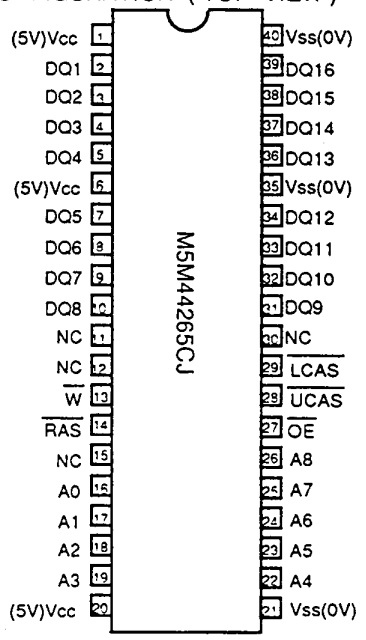
## APPLICATION

Microcomputer memory, Refresh memory for CRT, Frame Buffer memory for CRT

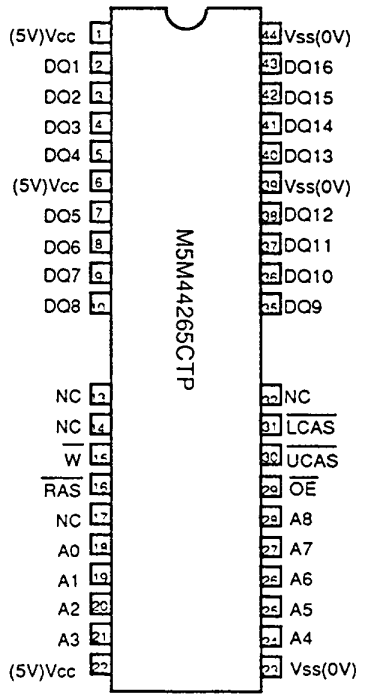
## PIN DESCRIPTION

| Pin Name | Function |
|---|---|
| A0-A8 | Address Inputs |
| DQ1-DQ16 | Data Inputs / Outputs |
| $\overline{RAS}$ | Row Address Strobe Input |
| $\overline{LCAS}$ | Lower Byte Control Column Address Strobe Input |
| $\overline{UCAS}$ | Upper Byte Control Column Address Strobe Input |
| $\overline{W}$ | Write Control Input |
| $\overline{OE}$ | Output Enable Input |
| Vcc | Power Supply (+5V) |
| Vss | Ground (0V) |

## PIN CONFIGURATION ( TOP VIEW )




Outline 40POK(400mil SOJ)




Outline 44P3W(400mil TSOP Nomal Bend)

NC: NO CONNECTION



M5M44265CJ,TP-5,-5S:under development

MITSUBISHI ELECTRIC

Mar. 1995

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## FUNCTION

In addition to Hyper Page Mode, normal read, write and read-modify-write operations the M5M44265CJ, TP provides a number of other functions,e.g.,,$\overline{RAS}$-only refresh,and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

| Operation | Inputs | | | | | Input/Output | |
|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{LCAS}$ | $\overline{UCAS}$ | $\overline{W}$ | $\overline{OE}$ | DQ1~DQ8 | DQ9~DQ16 |
| Lower byte read | ACT | ACT | NAC | NAC | ACT | Dout | OPN |
| Upper byte read | ACT | NAC | ACT | NAC | ACT | OPN | DOUT |
| Word read | ACT | ACT | ACT | NAC | ACT | DOUT | DOUT |
| Lower byte write | ACT | ACT | NAC | ACT | NAC | DIN | DNC |
| Upper byte write | ACT | NAC | ACT | ACT | NAC | DNC | DIN |
| Word write | ACT | ACT | ACT | ACT | NAC | DIN | DIN |
| $\overline{RAS}$ only refresh | ACT | NAC | NAC | DNC | DNC | OPN | OPN |
| Hidden refresh | ACT | ACT | ACT | NAC | ACT | DOUT | DOUT |
| $\overline{CAS}$ before $\overline{RAS}$ (Extended*) refresh | ACT | ACT | ACT | DNC | DNC | OPN | OPN |
| Self refresh* | ACT | ACT | ACT | DNC | DNC | OPN | OPN |
| Stand-by | NAC | DNC | DNC | DNC | DNC | OPN | OPN |

Note : ACT : active, NAC : nonactive, DNC : don' t care, OPN : open

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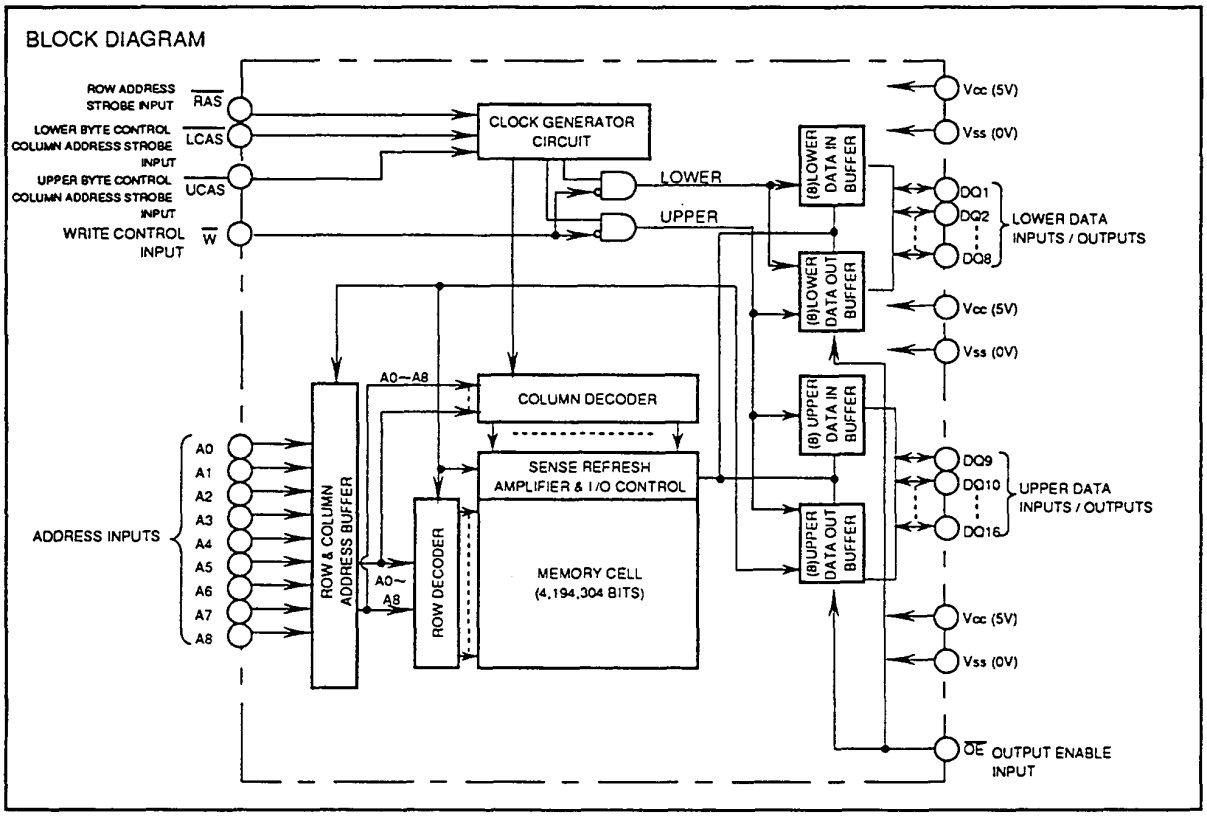
## BLOCK DIAGRAM



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